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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No. F0556 **PATENT**

In re Appellant:

	Ming-Ren Lin		
Serial No:	09/824,933	Art Unit:	2823
Filed:	April 03, 2001	Examiner:	Khiem D. Nguyen

For: SCRIBE LANE FOR GETTERING OF CONTAMINANTS ON SOI WAFERS AND GETTERING METHOD

APPEAL BRIEF

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This Appeal Brief is submitted, in triplicate, in the above-identified application in response to the final Office Action mailed August 01, 2003. Appellant's Notice of Appeal was mailed on September 09, 2003. Accordingly, Appellant's Appeal Brief is timely filed, with no extension of time.

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Dear Sir:

This Appeal Brief is submitted, in triplicate, in the above-identified application in response to the Office Action mailed August 01, 2003, in furtherance of the Notice of Appeal which was mailed on September 09, 2003.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., One AMD Place, Sunnyvale, California 94088.

II. RELATED APPEALS AND INTERFERENCES

Appellant is aware of no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-15 and 21-25 are presently pending in the Application. The Appendix contains a copy of all of claims 1-15 and 21-25.

IV. STATUS OF AMENDMENT

An amendment under 37 C.F.R. 1.116(a) was filed in this application, and the Examiner issued an Advisory Action. Thus, at the present time, there is no amendment pending.

V. SUMMARY OF INVENTION

Appellant's invention, in one embodiment, relates to a method of manufacturing a semiconductor device on a silicon-on-insulator (SOI) wafer, in which the SOI wafer includes a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane. Fig. 1, p. 5, lines 19-25. The method includes steps of forming at least one cavity through the silicon active layer in the at least one scribe lane (Figs. 4-6; p. 8, lines 19-29); forming at least one gettering plug in each cavity (Figs. 7-9; p. 10, line 26 to page 11, line 2), each gettering plug including doped fill material containing a plurality of gettering sites (p. 5, lines 27-30; p. 14, lines 18-20); and subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites (p. 14, line 28 to p. 15, line 21). Fig. 10 provides a schematic overview of the process of the present invention. The gettering plug includes doped fill material, the presence of which creates the gettering sites. The doped fill material may be provided either by implantation of the dopant into a filled cavity (steps S1003 and S1004 in Fig. 10; p. 11, lines 12-23) or by co-deposition of the dopant with the cavity fill material (step S1002 in Fig. 10; p. 11, lines 3-11).

The present invention addresses the problem of removing impurities which may be present in semiconductor devices such as SOI wafers. By providing gettering structures

in scribe lanes, the present invention provides a scribe lane gettering method which provides a significantly increased quantity and quality of gettering sites, and does so at a location which is in an otherwise underutilized area and thus does not consume valuable space on the SOI wafer. Use of doped polysilicon for the gettering structure provides a well-distributed large number of gettering sites and may be fabricated simply.

VI. ISSUES ON APPEAL

The claims on appeal stand rejected under 35 U.S.C. §§ 102(b). The issue in this appeal is:

APPELLANTS' CLAIMS 1-15 AND 21-25 WOULD NOT HAVE BEEN OBVIOUS OVER, AND HENCE ARE PATENTABLE OVER, HATTORI ET AL., U.S. PATENT NO. 6,252,294 IN VIEW OF MO ET AL., U.S. PATENT NO. 6,429,481, AND TSENG, U.S. PATENT NO. 5,677,222.

VII. GROUPING OF CLAIMS

Appellant's claims stand or fall together.

VIII. ARGUMENT

A. Hattori et al., U.S. Patent No. 6,252,294, Together with Mo et al., U.S. Patent No. 6,429,481, Fail to Disclose All the Limitations of Appellant's Independent Claims 1, 9 and 21, There is No Showing of Motivation to Combine and Modify the Prior Art, and There is No Reasonable Probability of Success; Therefore None of Claims 1-15 and 21-25 Would Have Been Obvious Over, and Hence All of the Claims Are Patentable Over These References.

Claims 1-15 and 21-25 stand rejected under 103(a) as obvious over Hattori et al., U.S. Patent No. 6,252,294, in view of Mo et al., U.S. Patent No. 6,429,481, and further in view of Tseng, U.S. Patent No. 5,677,222. The Examiner asserted that Hattori teaches some elements of the claimed invention, but admitted that Hattori et al. fails to teach all the features of the claimed invention. The Examiner cited and relied upon Mo et al., contending that Mo et al. remedies some of the admitted deficiencies of Hattori et al. The Examiner resorted to Tseng in order to allegedly find all of the features of Appellant's claimed invention. It is not possible to know from the statement of the rejections exactly

which claims are rejected over which asserted aspects of the cited references. However, Appellant respectfully traverses the rejections over Hattori et al. in view of Mo et al. and Tseng, in any combination, for the reasons set forth in detail herein. Appellant respectfully requests the Board to reverse the Examiner's rejection of Appellant's claims over the asserted combination of references.

In summary, as will be shown in detail in the following, Appellant submits that the asserted combination of references does not disclose all the features of Appellant's invention, that the disclosures of the references cannot properly be combined in accordance with the law of obviousness to yield Appellant's claimed invention as asserted by the Examiner, and that as a result the Examiner's rejection of Appellant's claims 1-15 and 21-25 cannot stand and should be reversed.

The Examiner's attempts to identify all of the features of Appellant's claims in the cited references are factually incorrect and the rejection is therefore without proper basis in law. In addition, failing to identify all of the features, the Examiner cannot have shown a reasonable expectation of success, and cannot have shown a motivation to have made the modifications of the teachings of the references which would be necessary to reach Appellant's claimed invention. Failing on all these points, Appellant respectfully submits that the Examiner failed to state either a factually or a legally correct *prima facie* case of obviousness.

(1) The Rejection.

The Examiner asserted that Hattori et al. teaches a process similar to that claimed by Appellant, but admitted that Hattori et al. fails to disclose each gettering plug comprising doped fill material containing a plurality of gettering sites and fails to disclose the doped fill material is polysilicon formed by LPCVD deposition of the silicon and the dopant in the cavity, and fails to disclose that the dopant ions are one or more selected from P, As, Sb, Bi, B, Al, Ga, In, He, Ne, Ar, Kr, Xe and Ge, as recited in various of Appellant's claims.

Admitting that Hattori et al. fails to disclose doped polysilicon gettering plugs, the Examiner resorted to Mo et al., asserting that Mo et al. discloses "gettering plugs

comprising doped fill material containing a plurality of gettering sites wherein the doped fill material is polysilicon formed by deposition of the polysilicon and the dopant in the cavity and that the dopant is P."

The Examiner also admitted that neither Hattori et al. nor Mo et al. discloses the embodiment in which the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and the dopant in the cavity. In order to remedy this deficiency of both the primary and secondary references, the Examiner resorted to Tseng, asserting that Tseng discloses the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and the dopant in the cavity, citing col. 5, line 63 to col. 6, line 2 and Fig. 15 of Tseng.

Finally, having assembled the selected disclosures from the prior art in order to allegedly find all of the elements of Appellant's claimed invention, the Examiner simply concluded "It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Hattori, Mo and Tseng to enable the doped fill material of Hattori to be formed."

The statement of the rejection and the contended factual basis therefor are deficient and in error. In addition, the rejection is legally faulty.

(2) Hattori et al.

Hattori et al. discloses forming gettering structures in which polycrystalline silicon is used. The only other material suggested by Hattori et al. for the getting material is silicon oxide. Col. 4, lines 44-45. This disclosure would not suggest use of a doped polysilicon instead of the disclosed materials. Hattori et al. simply fails to provide any basis whatsoever for modifying its specific teachings from the use of polysilicon or silicon oxide to the use of any other material. The Examiner failed to point out any such suggestion in Hattori et al. and Appellant is aware of none.

Thus, Hattori et al. fails to provide any motivation or suggestion to modify the disclosed polysilicon gettering plugs in any way, much less to suggest that they be modified by doping or by the addition of any specific dopants.

(3) Mo et al.

Mo et al. discloses forming a conductive gate electrode 28 which includes doped polysilicon. Mo et al. relates to conventional, non-SOI wafers. Mo et al. discloses doping polysilicon, but ***not*** for the purpose of forming a gettering plug. The conductive electrode 28 is not a gettering plug, and there is nothing whatsoever in Mo et al. to suggest use of the conductive electrode 28 as a gettering plug. No person of ordinary skill in the art would suggest that the conductive electrode 28 could be used for gettering or is a gettering plug.

There is nothing in Mo et al. which would provide any suggestion or motivation to take the disclosure relating to the conductive electrode 28 and to combine this with the disclosure of Hattori et al. in order to modify the gettering structures of Mo et al. in a way which would lead to Appellant's claimed invention. Appellant respectfully submits that the only way to make this combination is by means of improper hindsight reconstruction of Appellant's invention, using Appellant's disclosure and claims as a guide.

Mo et al. discloses nothing more than highly conventional doping of semiconductor materials to form conductive components such as the gate electrode 28, which is entirely conventional for forming *conductive* elements. Mo et al. fails to disclose or suggest that the conductive gate electrode 28, formed by doping a polysilicon structure, could act as a gettering plug, or that the process of doping the polysilicon structure could be used in forming a gettering plug.

The Examiner seized upon a passing mention of gettering in Mo et al. and contended this provides a basis to support his asserted combination. As pointed out in more detail below, the mere mention of gettering at col. 6, lines 48-51, following a disclosure relating to doping the polysilicon to form the conductive electrode 28, is not related to the conductive electrode 28 and fails to provide the requisite motivation to somehow apply this teaching to the unrelated disclosure of Hattori et al. The mention of gettering in Mo et al. is by way of contrast to the conventional doping of the silicon substrate for backside gettering in non-SOI devices, ***not*** as any teaching that the conductive electrode 28 could be used for gettering or that doped polysilicon could be

substituted for the polysilicon in the gettering structure of Hattori et al. The Examiner's reliance upon this passage is wholly erroneous and cannot provide the requisite factual basis for the conclusion of *prima facie* obviousness. Reliance on this passage can only result from use of improper hindsight, based on Appellant's disclosure, ***not*** on the teachings of the reference.

Furthermore, the Examiner failed to show any facts in support of the required showing of a reasonable expectation of success. The Examiner merely selected components without showing any evidence of how a person of skill in the art could derive a reasonable expectation of success in the asserted selection, combination and modification. For this additional reason, these are improper rejections.

Various elements of Appellant's claimed invention, found in the references and cited and relied upon by the Examiner, are variously available in the prior art, but always with significant differences, as discussed above. The significant differences require selection, combination and modification, for which there must be *both* a motivation *and* a reasonable expectation of success. Even if all the individual elements could be found in the cited references, there is still no teaching in any of the references to motivate and support the selection, modification and combination of these elements as was done by the Examiner to support the contention that Appellant's claimed invention would have been obvious. For this reason, the rejection of Appellant's claims is without proper basis in fact or law. Appellant respectfully requests the Examiner to withdraw the rejection of the presently claimed invention.

With respect to the mere passing mention of gettering in Mo et al., the Examiner cited col. 6, lines 39-51 and Fig. 1A of Mo et al. as the alleged support for the assertion that Mo et al. discloses "doped fill material containing a plurality of gettering sites....". The Examiner's asserted reading of the above-cited disclosure of Mo et al. is misleading because it selectively takes words out of context. The entire cited portion of Mo et al. at col. 6, lines 39-51 is reproduced here:

> Next, as shown in FIG. 4e, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. 4e). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. 4e). The polysilicon is then doped to n-type, e.g., by conventional $POCl_3$ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

As shown by the foregoing, the Examiner's selective, out-of-context reading of this disclosure of Mo et al. is clearly erroneous and is a factually incorrect statement of the disclosure. Mo et al. at no time discloses or suggests that the doped polysilicon of the gate electrode 28 contains a plurality of gettering sites or could be used for gettering.

The final sentence of the above disclosure relates to backside gettering only. It is distinct from the preceding sentences and includes no suggestion the disclosed doping to form the gate electrode has anything to do with gettering. The mention of gettering in the latter quoted sentence is the only mention of gettering at any time in the entire disclosure of Mo et al. The latter sentence relates only to backside gettering for non-SOI devices, and clearly shows that any gettering in Mo et al. is expected to occur into the substrate, not into the gate electrode 28. The latter sentence says nothing about adding dopants to form a polysilicon gettering plug. The latter sentence says that the backside of the wafer is conventionally stripped prior to doping to form semiconductor elements (i.e., source, drain), and refers only to a highly doped substrate which can be used for gettering, not to a doped gettering plug. As noted above, Mo et al. relates only to conventional, non-SOI wafers and devices, and there would be no need for gettering in the active region since backside gettering is available. The distinction between bulk silicon (non-SOI) and SOI wafers in terms of impurities and gettering is noted in Appellant's specification at page 1, line 29 to page 2, line 10.

Neither the above-quoted disclosure from Mo et al., nor any other disclosure in Mo et al., says or suggests anything about doping a polysilicon gettering plug, nor does it say or suggest anything that would lead a person of ordinary skill in the art to use doped polysilicon for a gettering plug.

The Examiner's contention that Mo et al. teaches "doped fill material containing a plurality of gettering sites..." is clearly in error and cannot provide the required factual basis for a *prima facie* obviousness rejection, because the reference simply does not disclose this. Mo et al. does not disclose gettering sites, does not use these terms, and no person of ordinary skill would understand this from the disclosure of Mo et al. Thus, there is nothing in either of Hattori et al. or Mo et al. which in any "hindsight-free" combination would have rendered obvious Appellant's invention, as claimed in independent claims 1, 9 and 21, and therefore any of the claims dependent upon these independent claims.

The cited references fail to disclose or suggest all the limitations of Appellant's claimed invention. Hattori et al. fails to disclose or suggest, and fails to provide any motivation whatsoever for, substitution of doped polysilicon or any other material except silicon oxide, for the gettering material. The disclosure of Mo et al. fails to provide any suggestion that a doped polysilicon material in a plug or trench used for a conductive electrode could be used for gettering. Tseng was cited only for showing LPCVD deposition of doped polysilicon. As in Mo et al., Tseng forms a conductive electrode from the doped polysilicon (Abstract; col. 6, lines 7-12, etc). Tseng fails to disclose or suggest gettering by the doped polysilicon; Tseng fails to even mention "getter" or "gettering". The disclosure of Tseng thus fails to remedy the shortcomings of Hattori et al. and Mo et al.

Not even by use of hindsight could the combined features of Appellant's invention be extracted from these cited references, since none of them disclose "forming at least one gettering plug in each said cavity, each said gettering plug comprising doped fill material containing a plurality of gettering sites". The references simply fail to disclose all the features of Appellant's claimed invention. Since the references fail to disclose all the features of the claimed invention, there can be no obviousness.

Since the references fail to disclose all the limitations of the claimed invention, there can be no motivation to make the claimed invention, and no obviousness.

Since the references fail to disclose all the limitations of the claimed invention and fail to provide any motivation, there can be no reasonable likelihood of success in making the alleged combination, and no obviousness.

Thus, the Office Action has stated none of the legally required elements of a case of *prima facie* obviousness. The rejection therefore cannot stand and must be withdrawn.

B. The Examiner Failed to State a Legally Proper *Prima Facie* Case of Obviousness.

The Examiner has failed to carry the burden of factually supporting the asserted *prima facie* obviousness, which is required under MPEP §2142. The rejection set forth in the present case is based upon clearly erroneous facts and fails to comport with the law. Thus, the rejection fails, both on a factual basis and on a legal basis, to state a *prima facie* case of obviousness. None of the legally required elements of a prima facie case of obviousness is present or has been shown in this case. Therefore, Appellant respectfully traverses this rejection, and respectfully requests the Examiner to reconsider and withdraw the rejections, which cannot stand.

In order to establish a prima facie case of obviousness, the Examiner must establish: (1) some suggestion or motivation either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) a reasonable expectation of success; and (3) that the prior art references must teach or suggest all the claim limitations. See MPEP 706.02(j)). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not be based on the applicant's (or appellant's) disclosure. *In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991).

In the present rejections, the Examiner merely selected, out of context, particular components from the cited references and then concluded that these components can be

combined and/or modified to render Appellants' claims obvious. These are, therefore, improper rejections. As set forth in MPEP §2143.01:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed.Cir. 1990).

In the present rejections, the Examiner failed to show any proper motivation for, i.e., the suggested desirability of, making the asserted selections, combinations and modifications in order to arrive at a combination of features similar to that recited in Appellants' claims. These are, therefore, improper rejections. As stated by the Federal Circuit:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. Under section 103, teachings of references can be combined *only* if there is some suggestion or incentive to do so. (Emphasis in original.)

ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 USPQ 929, 933 (Fed. Cir. 1984). The prior art of record fails to provide any such suggestion or incentive. The Examiner merely contended that the selected particular components of the references *could be* selected, combined or modified, on an ad hoc basis, and has not shown any teaching, suggestion or motivation to make the selections, combinations and modifications. Accordingly, Appellant respectfully submits that the Examiner erred as a matter of law in concluding that the claimed invention would have been obvious to one of ordinary skill in the art under section 103.

C. The Examiner Failed to Rebut Appellant's Arguments.

(1) The Final Office Action.

In the section of the final Office Action headed "Response to Appellant's Arguments" the Examiner attempted to rebut Appellant's argument that the *combined* references fail

to teach all the limitations of Appellant's claims by arguing in response to an argument not made by Appellant. Specifically, the Examiner "conceded" that "no one of the references teaches all the limitations of the independent claims". *This is not what Appellant argued.* Appellant stated then and continues to state now that the *combined* references fail to teach all the limitations of Appellant's claims. *In the both final Office Action and in the Advisory Action the Examiner failed to rebut this statement of fact by Appellant.* The Examiner simply persisted in his erroneous view of the disclosures of the cited references.

The Examiner admitted that he has failed to identify all of the features of Appellant's claimed invention, and in substance admitted to the use of hindsight, since the only way to make the asserted, necessary modification of the disclosures of the references is by improper use of hindsight. The Examiner stated at page 5 of the final Office Action:

> Hattori teaches the method of forming cavities, filling them with fill material and forming condition to getter impurities. Mo is combined for the limitation for forming a doped polysilicon plug. Although as the applicant cites, the effect of doping for enhanced gettering may refer to bulk polysilicon, the physical effect would be the same.

This fails to show all the features of Appellant's claimed invention and fails to identify any motivation for the asserted combination of reference features. At no time do the references disclose or suggest and at no time does the Examiner show any teaching that the "doped polysilicon plug" of Mo could be used as a gettering plug in addition to or instead of its sole disclosed use as the gate electrode 28. At no time does the Examiner show any factual basis for the assertion in the final sentence of the above-quoted statement. Nor does the Examiner show how this statement flows from the references. The Examiner's contentions can only be the result of improper hindsight, since none of the references make any statement which would lead a person of ordinary skill in the art to make this connection.

The Examiner's other arguments fail to meet the point of Appellant's arguments and facts. For example, the Examiner asserted that "one cannot show non-obviousness by merely attacking references individually where references are based on combinations of references." Appellant has not made any such argument. Rather, Appellant has repeatedly pointed out, and the Examiner has repeatedly failed to rebut, that the *combined* references fail to teach or suggest all the features of Appellant's claimed invention. Based on the foregoing, the rejections cannot stand, since there is no *prima facie* obviousness.

(2) The Advisory Acton.

Similarly, in the Advisory Action mailed August 27, 2003, the Examiner again attempted to assert that Mo et al. teach that the gate electrode 28 is a gettering plug containing a plurality of gettering sites. This is simply not true. It is an incorrect statement of the disclosure of Mo et al. In the Advisory Action, the Examiner stated:

> In response to applicant's argument that Hattori et al. and Mo et al. fail to teach wherein each gettering plug comprising doped fill material containing a plurality of gettering sites, examiner disagree. Hattori teaches the method of forming cavities, filling them with fill material and forming condition to getter impuritie (Office Action mailed 08/01/2003, pages 2-3). Mo teaches that each gettering plug (FIG. 1A, 28) comprises doped fill material containing a plurality of gettering sites wherein the doped fill material is polysillcon formed by deposition of the polysilicon and the dopant in the cavity (FIG. 1A, 14) and wherein the dopant ion is phosphorus (col. 6, lines 39-51 and FIG. 1A).

This statement repeats the most egregious of the Examiner's erroneous assertions of fact, which is the contention that Mo et al. teaches a gettering plug, citing Fig. 1A and reference numeral 28. Fig. 1A of Mo et al., and the description thereof, clearly identifies "28" as "gate electrode 28". While it is correct that the gate electrode 28 fills a trench and therefore might be considered to constitute a "plug", there is no disclosure or suggestion in Mo et al. that the gate electrode 28 is a gettering plug, or that it contains gettering sites. It is clearly

erroneous that Mo et al. teach or suggest use of doping polysilicon in a cavity for use as a gettering plug. As noted elsewhere in this Brief, Mo et al. clearly contemplate backside gettering into the doped substrate, not use of the gate electrode 28 as a gettering structure.

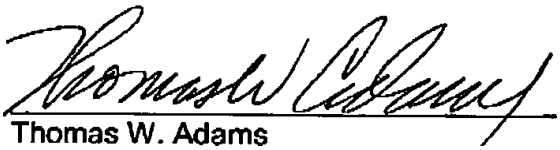
Thus, the Examiner failed to rebut Appellant's arguments and statements of fact relating to the disclosures of the cited references. For this additional reason, the rejection of Appellant's claims is erroneous and should be reversed. Accordingly, Appellant respectfully requests the Board to reverse the Examiner's rejections.

IX. CONCLUSION

For all these reasons, the rejection of Appellant's claims 1-15 and 21-25 under 35 U.S.C. §103(a) should be reversed because the asserted combination of references would not have rendered obvious Appellants' claimed invention at the time the invention was made. Appellants respectfully request reversal of the Examiner's rejections of Appellants' claimed invention under Section 103(a).

In the event issues remain in the prosecution of this application, Appellants request that the Examiner telephone the undersigned attorney to expedite consideration and/or allowance of the application. Should a Petition for Extension of Time be necessary for the present Appeal Brief to be timely filed (or if such a petition has been made and an additional extension is necessary) petition therefor is hereby made and, if any additional fees are required for the filing of this paper, the Commissioner is authorized to charge those fees to Deposit Account #18-0988, Docket No. F0556, AMDSP0448US.

Respectfully submitted,
RENNER, OTTO, BOISSELLE & SKLAR



Date: September 11, 2003

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1-15, 21-25 (1, 9, 21)

APPENDIX:

CLAIMS ON APPEAL

100 501

1. A method of manufacturing a semiconductor device on a silicon-on-insulator wafer including a silicon active layer (102) having at least two die pads (104) formed thereon, the at least two die pads separated by at least one scribe lane (106), comprising the steps of:

forming at least one cavity (120A) through the silicon active layer in the at least one scribe lane;

forming at least one gettering plug (108) in each said cavity, each said gettering plug comprising doped fill material (122) containing a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

2. The method of claim 1, wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and a dopant in the cavity.

3. The method of claim 2, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

4. The method of claim 3, wherein the dopant is phosphorus.

5. The method of claim 1, wherein the step of forming at least one cavity further comprises forming a sidewall (114) liner in the cavity.

6. The method of claim 1, wherein the gettering plug extends down through the silicon active layer, and contacts a dielectric (110) insulation layer on the wafer.

7. The method of claim 1, wherein the gettering plug extends down through both a silicon active layer and a dielectric insulation layer on the wafer.

8. The method of claim 7, wherein in the gettering step gettered impurities migrate into a silicon substrate layer below the dielectric insulation layer.

9. A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming at least one cavity through the silicon active layer in the at least one scribe lane;

filling the cavity with a fill material;

adding at least one dopant to the fill material to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

10. The method of claim 9, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

11. The method of claim 9, wherein the step of forming at least one cavity further comprises forming a sidewall liner in the cavity.

12. The method of claim 9, wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation.

13. The method of claim 9, wherein the gettering plug extends through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

14. The method of claim 9, wherein the gettering plug extends through both the silicon active layer and a dielectric insulation layer on the wafer.

15. The method of claim 14, wherein in the gettering step gettered impurities move into a silicon substrate layer below the dielectric insulation layer.

21. A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer, buried oxide layer and a silicon substrate, the silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming a plurality of cavities through the silicon active layer and the buried oxide layer to the silicon substrate in the at least one scribe lane;

filling the cavities with a fill material;

implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

22. The method of claim 21, wherein in the gettering step, gettered impurities move into the silicon substrate.

23. The method of claim 21, wherein the wafer comprises a plurality of adjacent die pads and a single scribe lane separates each die pad from the adjacent die pads.

24. The method of claim 23, wherein the scribe lane comprises a single row of gettering plugs, a pair of parallel rows of gettering plugs or a pair of parallel gettering trenches.

25. The method of claim 21, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.